PATENT APPLICATION

Sheet 1 of 1

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 10030972-1	SERIAL NO. 10/775,960
	APPLICANT Steinbach et al.	
	FILING DATE	GROUP

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIAL	*	DOCUMENT NUMBER	DATE	NAME
DC		6,545,545	4/8/2003	Fernandez-Texon

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	NAME	TRANSLATION YES	TRANSLATION NO

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

DC		DUNNING, GARCIA, LUNDBERG, NUCKOLLS, An all-Digital Phase-Locked Loop with 50-Cycle Lock Time Suitable for High-Performace Microprocessors, IEEE Journal of Solid-State Circuits, Vol. 30, No. 4, April 1995, pp.412-422.
DC		ANAND, RAZAVI, A 2.75 Gb/s CMOS Clock Recovery Circuit with Broad Capture Range, IEEE ISSCC 2001 Degest, p.214.
DC		NOGUCHI, TATEYAMA, OKAMOTO, UCHIDA, KIMURA, and TAKAHASHI, A 9.9G-10.8Gb/s Rate-Adaptive Clock and Data-Recovery with No External Reference Clock for WDM Optical Fiber Transmission, IEEE ISSCC 2002 Digest, p.252.

EXAMINER	DATE CONSIDERED
Kim Kent	12/23/05

* **Copies of these references are not enclosed pursuant to 37 CFR 1.98(d). (See accompanying IDS)**